SYSTEM DESIGN
USING THE INS8073
HIGH LEVEL LANGUAGE PROCESSOR

BY

RON PASQUALINI

INTRODUCTION

The INS8073 is a one chip computer which executes a high level language. The language executed is NIBL2, which stands for National Industrial Basic Language, Version 2. NIBL2 is an enhanced version of NIBL, a BASIC like high level language which is executable on the INS8060 processor. Since the INS8060 does not have internal ROM, the NIBL interpreter must reside in 4k bytes of external memory, which is usually ROM or EPROM. The INS8073 completely eliminates the need for this external memory, because the NIBL2 interpreter is stored in ROM which is located inside the INS8073. This reduces system package count and interconnect, resulting in a less expensive, more reliable system.

Writing programs in NIBL2 offers several important advantages over writing programs in assembly language. These include:

* Elimination of the need for memory consuming EDITOR, ASSEMBLER and DEBUG programs. All of these functions are built into NIBL2.

* Purchase of an expensive development system is not required. Programs may be written and debugged using a small, inexpensive system similar to the one described in the succeeding paragraphs.

* Fast and simple program debug. Program execution may be suspended, variables and other parameters examined/altered, errors corrected, and execution resumed at the point where it was suspended — all without the need to reassemble, recompile or reload the program. (Since NIBL2 programs are interpreted, they do not have to be assembled or compiled.)

* NIBL2 programs can be written up to 10 times faster than equivalent assembly language programs due to the power of the NIBL2 language, its English-like simplicity, and built-in edit/debug capability. NIBL2 programs are also easier to maintain because they are self-documenting.

* Since NIBL2 programs are relocatable, they may be loaded and executed anywhere in memory without modification. This also implies that NIBL2 program ROMs will not become obsolete if their address locations must be changed in the final system. (Most assembly language ROM programs are not relocatable; they can only be executed at the memory locations where they were assembled.)

* NIBL2 program memory can be quickly checked for valid code because NIBL2 programs are stored as a sequence of ASCII characters. (Executable assembly language programs are considerably more difficult to check because they are stored in memory as a sequence of binary numbers.)

NOTE:

FOR A DETAILED DESCRIPTION OF THE INS8073 AND THE NIBL2 LANGUAGE, REFER TO THE INS8073 DATA SHEET AND THE NIBL2 USER'S MANUAL

MINIMUM RAM BASED SYSTEM

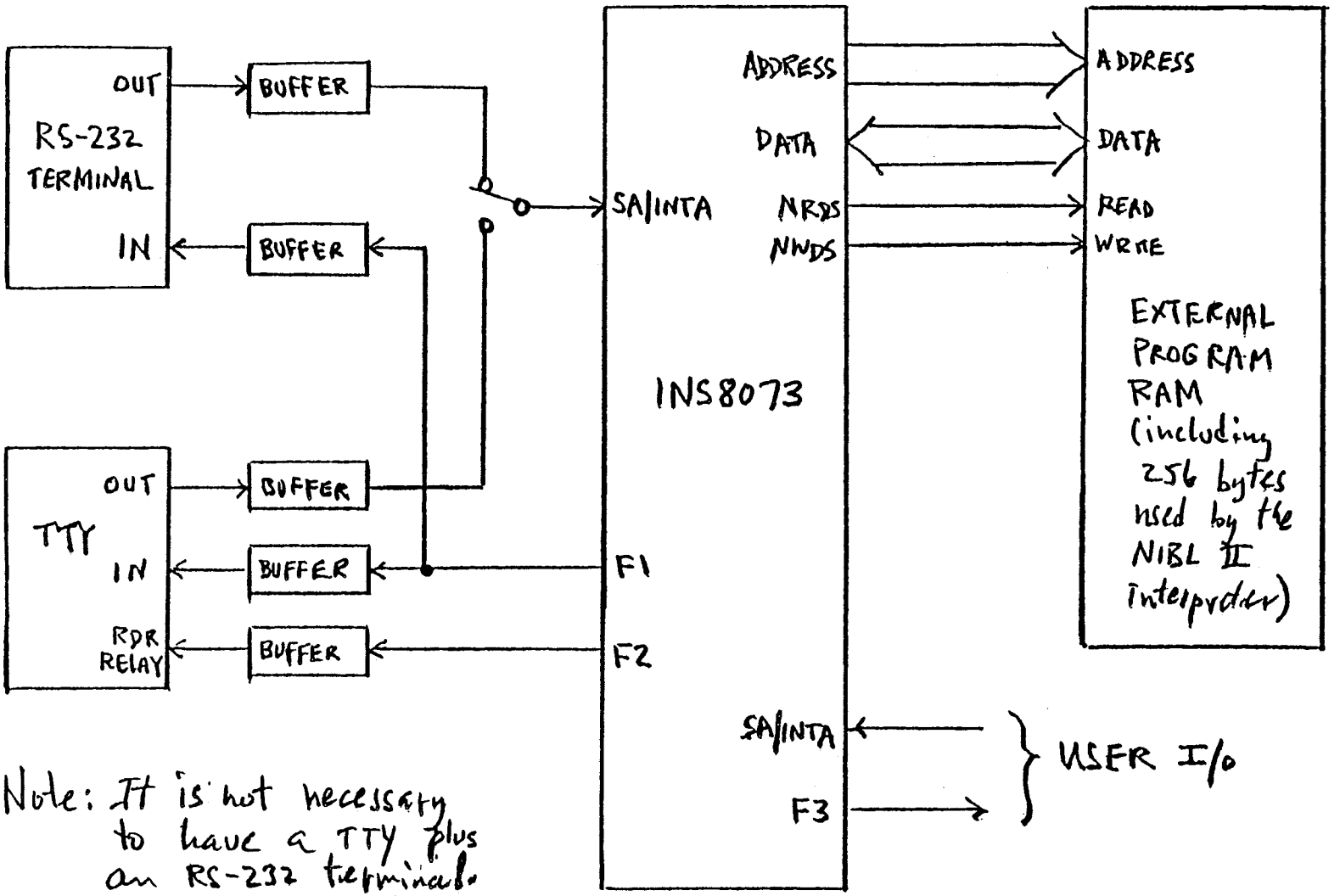
A minimum RAM based system appears in fig 1. As shown, the system simply consists of the INS8073 plus sufficient external RAM to store the user's program, including 256 RAM bytes required by NIBL2. In order to connect the INS8073 to a TTY or terminal, only simple buffers must be added to translate the serial I/O signals to RS-232 and/or current loop levels. One kilobyte of external RAM is sufficient to store a typical 30-60 line program.

LOCATION OF EXTERNAL RAM

External RAM may be located anywhere in the address range X'1000 to X'FFBF. (This represents approximately 60,000 bytes.) Following power up or after a 'NEW' command has been entered, NIBL2 will automatically determine the location and amount of external program RAM which is present. (External program memory must be contiguous). After the limits of external RAM have been determined, NIBL2 will warn the user if he attempts to enter program lines beyond these limits.

SAVING A RAM RESIDENT PROGRAM

When a TTY is employed for program input/output, a RAM resident program may be saved on paper tape for future use. This is accomplished by simply typing the NIBL2 'LIST' command and turning on the paper tape punch before a carriage return is



Note: It is not necessary to have a TTY plus an RS-232 terminal. Either one may be omitted.

FIG 1 MINIMUM RAM BASED SYSTEM

5/4/79 RP

entered. Since NIBL2 treats paper tape input exactly the same as keyboard input, a paper tape resident program may be entered into RAM by simply inserting the paper tape into the tape reader. In order to assure that all characters are properly accepted, NIBL2 controls the paper tape reader relay as shown in fig. 1.

Alternate approaches to to saving RAM resident programs include audio cassette tape storage and EPROM storage. These methods will be discussed in subsequent sections.

MINIMUM ROM/EPROM BASED SYSTEM

The INS8073 may be used in real time control applications where a terminal is not normally present. For these applications a previously written control program can be stored in ROM/EPROM. Program execution will be automatically initiated following power up if external ROM is located at memory location X'8000. This occurs because NIBL2 examines this location following power up in order to determine whether or not it contains ROM. If ROM is present at X'8000, execution of the ROM program which is present will automatically commence.

A minimum ROM based system appears in fig 2. As shown, the system consists of three devices: the INS8073, a program ROM or EPROM, and at least 256 bytes of RAM.

INPUT/OUTPUT CAPABILITY OF THE MINIMUM RAM AND ROM BASED SYSTEMS

As shown in fig. 1, in a RAM based system programs are transferred to/from the terminal via the INS8073 F1 output and SA/INTA input. (F2 is used to enable/disable the reader relay for TTY paper tape I/O.) Thus the non-terminal related I/O resources of the minimum RAM based system consist of one sense/interrupt input (SB/INTB), and one flag output (F3). This capability is sufficient to implement one serial I/O data channel, or to control one output in response to a single input.

The I/O capability of the minimum ROM based system shown in fig 2 consists of two sense/interrupt inputs (SA/INTA and SB/INTB), and three flag outputs (F1, F2 and F3). These five I/O lines can be utilized to sense and control a wide variety of physical variables, including pressure, temperature, displacement, RPM, torque, etc. Each of the three flag outputs can supply sufficient drive current to directly drive Darlington type relay drivers, hammer drivers, lamp drivers, etc.

The SA/INTA and F2 pins may be inhibited from performing their designated terminal functions in a ROM/EPROM based system by simply including the NIBL2 statement "ON 1,0" in the user's program. After this statement is executed, these pins may be utilized for general purpose I/O. (In this case the user should not employ any 'INPUT' statements in the program.) When employed as a sense input, the SA/INTA pin may be examined and tested via the NIBL2 'STAT' variable.

If the user's ROM based program is not required to supply output

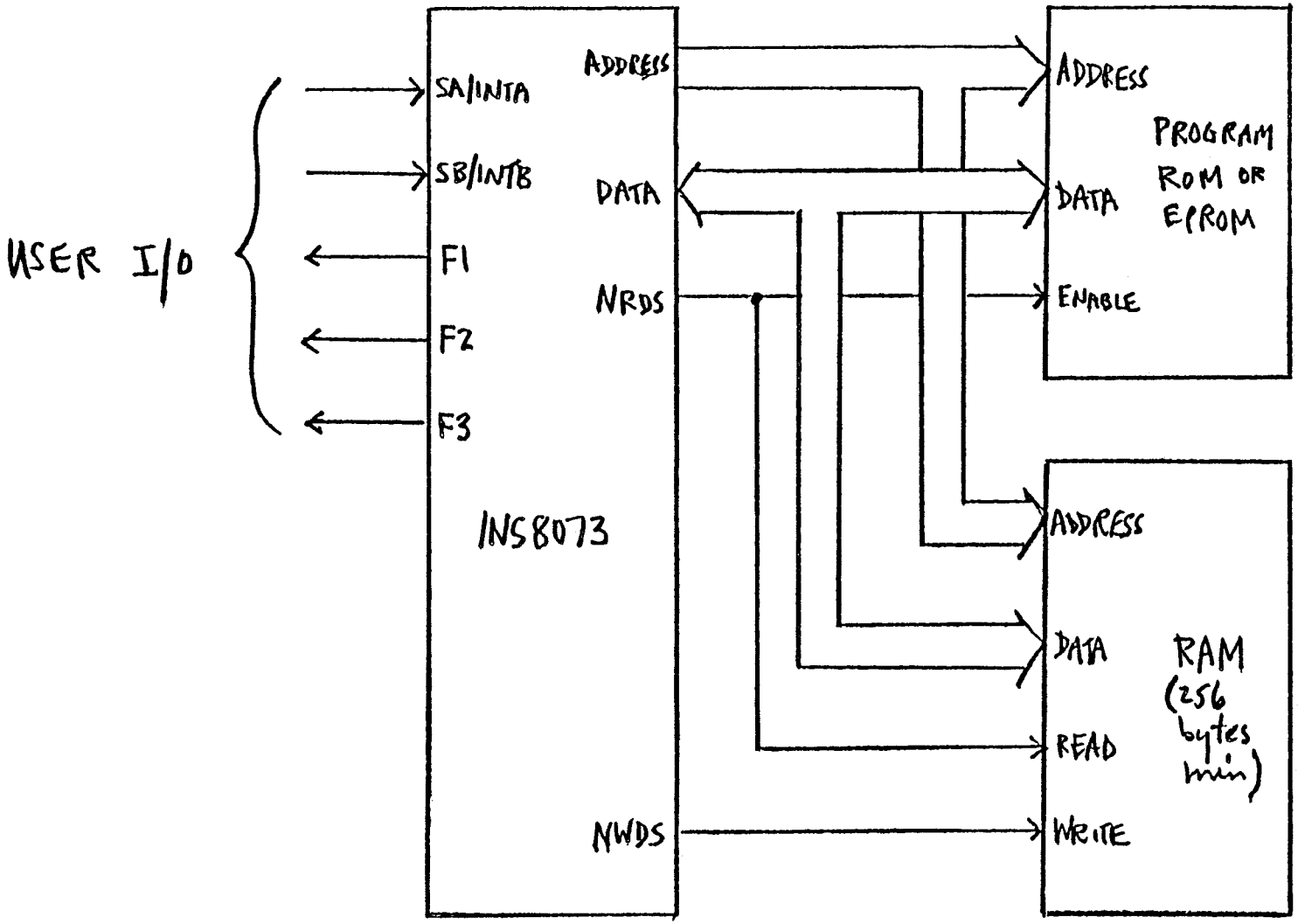


FIG 2 MINIMUM ROM BASED SYSTEM

5/4/79 RP

to a terminal, the F1 flag may also be employed as a general purpose output.

EXPANSION OF I/O CAPABILITY

The I/O capability of the INS8073 may be readily expanded via several methods. The best approach for any given system will depend upon the number and type of inputs/outputs to be sensed/controlled.

Input/output devices are usually "memory mapped". This implies that inputs and outputs are treated as locations in memory. These locations may be read in order to receive input, and written in order to supply output. Address decoding of I/O locations may be performed in many ways, depending upon the type of I/O hardware to be decoded.

Fig. 3 shows an example of how to expand the I/O capability of the minimum ROM based system shown in fig. 2. Although the system shown in fig. 3 consists of only 4 LSI devices, it contains a complete high level language computer and control program, plus 37 I/O lines. Thirty-two of these lines come from the I/O ports present on the INS8154s. Each port line may be individually programmed as an input or an output, under software control. Any line or port may be read or written via the NIBL2 '@' operator.

In addition to providing I/O expansion capability, the two INS8154s shown in fig. 3 also provide the 256 RAM bytes required by the NIBL2 interpreter.

In those systems where serial input/output of programs is not desirable, the TTY or terminal which is normally required for this purpose may be eliminated. This can be accomplished by substituting user written external subroutines for the internal input/output subroutines normally called by NIBL2. (Refer to the NIBL2 USER'S MANUAL for additional details.) By supplying external I/O subroutines, the user can directly interface the INS8073 to keyboards, printers, scanned displays, CRTs, etc.

REAL TIME CONTROL FEATURES OF NIBL2

NIBL2 provides several software features which make it ideal for use in real time control applications. These features include the ability to respond to interrupts via the 'ON' statement; the ability to execute high speed assembly language subroutines via the 'LINK' statement; and the ability to specify real time delays via the 'DELAY' statement. (Refer to the NIBL2 USER'S MANUAL for additional details.)

DESIGN SPECIFICATIONS FOR AN INS8073 BASED SYSTEM

The design of an INS8073 based system is quite straightforward. Using only a small number of ICs, an extremely powerful and flexible system can be easily developed. In order to illustrate

5/4/7 RP

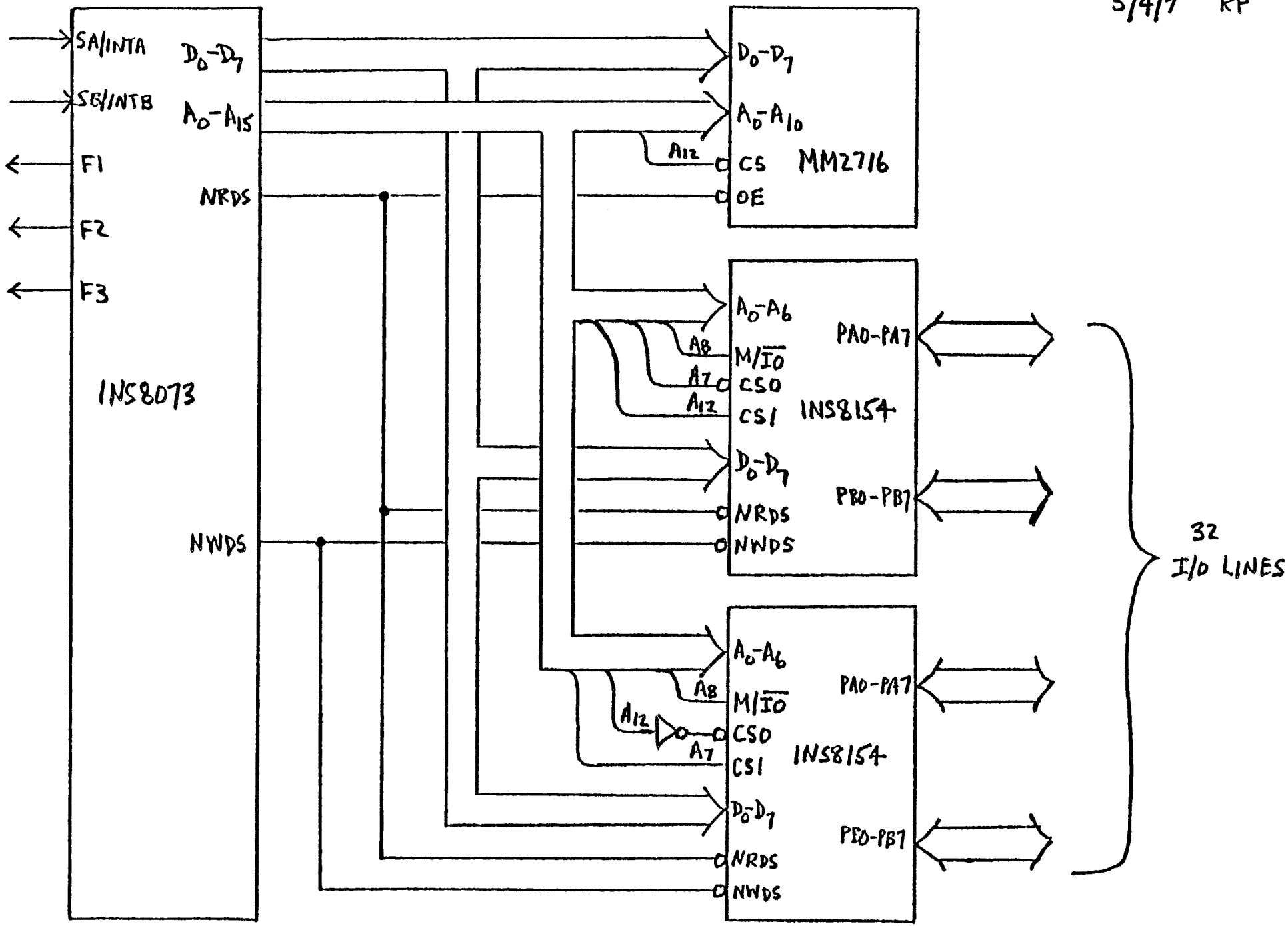


FIG 3 I/O EXPANSION OF THE MINIMUM ROM BASED SYSTEM

this point, we shall proceed to design a system which must satisfy all of the following requirements:

* The system shall allow the user to enter, debug and execute RAM based NIBL2 programs up to 150 lines in length.

* The system shall directly interface to an RS-232 terminal and to a TTY for program entry and debug. Multiple data rates (110, 300, 1200 and 4800 Baud) shall be supported.

* The system shall directly interface to an inexpensive audio cassette recorder for storage/retrieval of NIBL2 source programs and assembly language subroutines.

* The system shall directly interface to a "host" computer (via RS-232 and paper tape) for downloading of NIBL2 source programs and assembly language subroutines. Data transfer rates up to 4800 Baud shall be supported.

* The system shall allow the user to transfer RAM resident programs into EPROM and vice versa.

* The system shall allow the contents of one EPROM to be copied to another EPROM.

* The system shall allow an EPROM program to be run in a real time control application where a terminal is not present.

* The system shall have ample I/O capability which is flexible enough to interface to most user systems.

* The system shall provide the user with "scratchpad" RAM for use when assembly language subroutines are invoked via the 'LINK' statement.

* The system shall support at least two interrupts.

* The entire system shall fi on a single PC card no larger than 5"X7".

* The system shall satisfy all design requirements at minimum cost, using a minimum number of ICs. Expansion of the 'minimum' system shall be accomplished via simple addition of 'optional' RAM, EPROM and I/O devices directly on the PC card.

Although meeting all of the above requirements may at first seem difficult, these objectives are easily attainable, using minimal hardware external to the INS8073, as shown in the following paragraphs.

A system which meets all of the foregoing design requirements is shown in fig 4. The type, designation and function of each IC shown is as follows:

IC TYPE	IC DESIG	IC FUNCTION
INS8073	U1	NIBL2 processor
MM2114	U2,U3	U2 and U3 provide 1K bytes of static RAM. (Each MM2114 provides 1KX4 bits.)
74LS368	U4A	Inverter for TTY input interface.
	U4B	Inverter for TTY reader relay interface.
	U4C	Inverter for RAM address mapping logic.
	U4D	Inverter for power-on reset of INS8255A.
	U4E,U4F	TRI-STATE inverters for selection of multiple Baud rates.
74LS02	U5A	2 input NOR gate. Used for address mapping of the EPROM programmer.
	U5B	2 input NOR gate. Used to select interrupt source(s) to INS8073.
	U5C	2 input NOR gate. Used in Baud rate selection logic.
	U5D	2 input NOR gate. Used for address mapping of the INS8154.
LM747	U6A	The LM747 is a dual OP amp. U6A buffers the positive/negative voltage levels received from the RS-232 compatible input to the TTL levels required by the INS8073.
	U6B	U6B buffers the TTL levels generated by the INS8073 to the positive/negative voltage levels required to drive the RS-232 compatible output.
74LS123	U7A	The 74LS123 is a dual one shot. U7A provides adequate address/data

		setup time to program the MM2716 EPROM.
	U7B	U7B provides the 50 msec programming pulse which is required to write data into the MM2716 EPROM.
74LS00	U8A,B,C	U8 is a quad NAND gate. U8A, U8B and U8C are used in the Baud rate selection logic.
	U8D	Used in the RAM address mapping logic.
74LS139	U9	Dual 2 line to 4 line decoder with active low outputs. Provides address mapping for RAM, EPROM and I/O ICs.
MM2114	U10–U15	Provide an additional 3K bytes of optional RAM program memory.
MM2716	U16,U17	Provide up to 4K bytes of optional EPROM program memory. (Each MM2716 contains 2K bytes.)
INS8255A	U18	Optional Programmable Peripheral Interface chip. Provides 24 I/O lines which may be used to interface with the user's system. I/O pins may be programmed as inputs, outputs or bidirectional, including the required handshaking signals. (Refer to the INS8255A data sheet for additional information.)
INS8154	U19	Optional 128 byte RAM/IO chip. Provides 128 bytes of scratchpad RAM for use in assembly language subroutines. Also provides 16 I/O lines which may be individually programmed as input or output, including strobed mode with handshake. (Refer to INS8154 data sheet for additional information.)

Note from the above tabulation that the 'minimum' system consists of only 9 ICs, U1 - U9, plus a few discrete components. Together they provide 1K bytes of RAM program memory, an RS-232/TTY interface, an audio cassette interface, an MM2716 EPROM programmer, automatic Baud rate selection and complete decoding for the fully expanded system. The fully expanded system consists of 19 ICs.

ADDRESSING REQUIREMENTS / CAPABILITIES OF EACH SYSTEM COMPONENT

Each of the system components shown in fig. 4 must be assigned to address locations in memory. The built-in address decoding capability of each system component can be summarized as follows:

* 4K Bytes of RAM

  Each of the 4 pairs of MM2114 chips fully decodes 10 bits and can be selected via one active low select line per pair.

* 4K Bytes of EPROM

  Each of the 2 MM2716 EPROMs fully decodes 11 bits and provides 2 active low select lines per device for reading of data.

* INS8255

  The INS8255 contains 3 I/O ports and 1 control word register, all of which are decoded on-chip via 2 address input lines. The device is enabled via a single active low select line.

* INS8154

  The INS8154 contains 128 bytes of RAM, 2 I/O ports and 2 data direction registers, all of which are decoded on-chip via 8 address lines. The device is enabled via one active high select line and one active low select line.

* BAUD RATE SELECTION LOGIC

  The INS8073 selects the Baud rate by reading the contents of memory location X'FD00. In order to program the Baud rate, this location must be decoded via external logic, and the appropriate logic levels supplied on data lines 1, 2 and 7. (Refer to the RS-232 / TTY INTERFACE section for additional details)

* EPROM PROGRAMMER

  In order to program an MM2716 EPROM, address/data are supplied by the INS8073 to the MM2716 socket U16 in fig. 4. When VPP=+25V and address/data are valid, a single byte may be written by providing a 50 msec programming pulse to pin 18 while the chip is deselected via a logic 1 on pin 20. A byte which has been written may be subsequently read by simply supplying the correct address and providing a logic 0 on pin 20. (Refer to MM2716 data sheet for additional details)

MEMORY MAPPING CONSTRAINTS FOR ALL SYSTEM COMPONENTS

The components described above can be mapped into memory in a variety of ways. The system constraints we shall impose upon this mapping are the following:

1) The decoding hardware shall be implemented using a minimum number of low cost ICs. This implies that the system components will be only partially decoded, resulting in multiple images of each component in memory.

2) Although multiple memory images of each system component may be present, the mapping hardware shall be designed such that it is impossible to enable more than one system component at a time. This restriction eliminates the possibility of causing a data bus conflict as the result of a programming error. (A data bus conflict could cause transmittal/receipt of invalid data.)

3) NIBL2 program RAM shall be decoded as a contiguous block so that the INS8073 can successfully identify the beginning and end of the program RAM which is actually present.

4) The RAM and I/O ports of the INS8154 shall be located in the address range X'FF00 - X'FFBF. This will allow INS8073 assembly language subroutines to address the INS8154 using the DIRECT addressing mode. (Use of DIRECT addressing eliminates the need to dedicate or multiplex a pointer in order to address the INS8154. For additional details on DIRECT addressing, refer to the INS8070 data sheet.)

5) When on-card EPROM is present, it shall be located starting at address X'8000. This will allow the system to be used in real time control applications where a terminal is not present.

All of the above constraints are satisfied by the memory assignment shown in fig. 5 and fig. 6. Fig 5 shows how the 64K addressing space of the INS8073 is to be partitioned. Fig. 6 shows the address bits (in bold face type) which are actually decoded by the hardware shown in fig. 4, resulting in multiple (but not overlapping) memory images of each component. The locations of these multiple images are also shown, with address bits A12 - A15 specifying one of 16 possible memory 'pages'. Each page contains 4K bytes.

SYSTEM GENERATED INTERRUPTS

The NIBL2 interpreter supports interrupts via the "ON" statement in conjunction with the "STAT" variable. The statement "STAT=STAT OR 1" should be executed before the SA/INTA or SB/INTB interrupts can be serviced. This statement will enable both interrupts at the "hardware" level, but not at the "software"

HEX ADDRESS	MEMORY CONTENTS
0000 08FF	INS8073 ON-CHIP NIBL II INTERPRETER
	⋮
1000 13FF	RAM 0 (1K BYTES)
1400 17FF	RAM 1 (1K BYTES)
1800 13FF	RAM 2 (1K BYTES)
1C00 1FFF	RAM 3 (1K BYTES)
2000 27FF	MM2716 EPROM PROGRAMMER
	⋮
8000 87FF	ROM 0 (2K BYTES)
8800 8FFF	ROM 1 (2K BYTES)
	⋮
F700 F703	INS 8255A
FD00	⋮ BAUD RATE SELECT ⋮
FF00 FF7F	INS8154 RAM (128 BYTES)
FF80 FFA4	INS8154 I/O PORTS/CONTROL
	⋮
FFC0 FFFF	INS8073 ON-CHIP RAM (64 BYTES)

FIG 5 PARTITIONING OF THE INS8073 64K ADDRESSING SPACE

5/5/79 RP

5/7/79 RP

← ADDRESS BITS →																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPONENT
0	**0**	**1**	**0**	0	B	B	B	B	B	B	B	B	B	B	B	EPROM PROGRAMMER (X'2000-X'27FF)
0	**1**	**1**	**1**	**0**	**0**	B	B	B	B	B	B	B	B	B	B	RAM 0 (X'1000-X'13FF)
0	**1**	**1**	**1**	**0**	**1**	B	B	B	B	B	B	B	B	B	B	RAM 1 (X'1400-X'17FF)
0	**1**	**1**	**1**	**1**	**0**	B	B	B	B	B	B	B	B	B	B	RAM 2 (X'1800-X'1BFF)
0	**1**	**1**	**1**	**1**	**1**	B	B	B	B	B	B	B	B	B	B	RAM 3 (X'1C00-X'1FFF)
1	**0**	**0**	**0**	**0**	B	B	B	B	B	B	B	B	B	B	B	ROM 0 (X'8000-X'87FF)
1	**0**	**0**	**0**	**1**	B	B	B	B	B	B	B	B	B	B	B	ROM 1 (X'8800-X'8FFF)
1	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	B	B	INS8255A (X'F700-X'F703)
1	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	BAUD RATE SELECT (X'FD00)
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	B	B	B	B	B	B	B	B	INS8154 (X'FF00-X'FF7F)

NOTES: 1) "B" REFERS TO ADDRESS BIT WHICH MAY BE "0" OR "1"
2) BITS WHICH ARE ACTUALLY DECODED BY THE HARDWARE SHOWN IN FIG 4 APPEAR IN BOLDFACE TYPE

DECODING ONLY THE ADDRESS BITS SHOWN IN BOLDFACE TYPE RESULTS IN THE FOLLOWING MULTIPLE MEMORY IMAGES OF EACH COMPONENT:

COMPONENT		MEMORY PAGE
EPROM PROGRAMMER	—	0, 2, 4, 6
4K RAM	—	1, 3, 5, 7
4K ROM	—	8, A, C, E
INS8255A	—	9, B, D, F & $A_{11}=0$
BAUD RATE SELECT	—	9, B, D, F & $A_{11}=1$ & $A_9=0$
INS8154	—	9, B, D, F & $A_{11}=1$ & $A_9=1$

FIG 6 ADDRESS BIT DECODING FOR THE SYSTEM SHOWN IN FIG 4

level. The statement "STAT=STAT AND #FE" will disable both interrupts at the hardware level. Both interrupts are automatically disabled at the hardware level following VCC power on or after the reset (NRST) pin has been activated.

Interrupts may be enabled at the software level via the "ON" statement. For example, if the SA/INTA service subroutine begins on line number 500, execution of the statement "ON 1,500" will cause control to be transferred to this subroutine in response to an interrupt received on the SA/INTA line. Similarly, if the SB/INTB service subroutine begins on line number 600, execution of the statement "ON 2,600" will cause control to be transferred to this subroutine in response to an interrupt received on the SB/INTB line.

The SA/INTA interrupt may be independently disabled, at the software level, by executing the statement "ON 1,0". Similarly, the SB/INTB interrupt may be independently disabled, at the software level, by executing the statement "ON 2,0".

When employed as interrupt inputs, both SA/INTA and SB/INTB are trailing edge triggered. Edge triggered interrupts offer the advantage of not requiring an interrupt acknowledge signal in order to remove the interrupt service request, as required by level triggered interrupts.

If interrupts are disabled, the the SA/INTA and SB/INTB pins may be employed as general purpose sense inputs which may be examined via the NIBL2 'STAT' variable.

As shown in fig. 4, interrupts generated by the INS8154 and/or INS8255 may be connected, at the user's discretion, to the SB/INTB pin of the INS8073. When this is done, the INS8073 SB/INTB pin may be used to detect interrupts under control of the user's NIBL2 program.

RS-232 / TTY INTERFACE

The terminal Baud rate is established when the INS8073 is initialized. Initialization is automatically accomplished at VCC power on by R1 and C1 in fig. 4. (Depressing switch S1 will also cause the INS8073 to be initialized.) The Baud rate is jumper selectable as follows:

E16-E17 JUMPER	E18-E19 JUMPER	D7	D2	D1	BAUD RATE
PRESENT	PRESENT	1	1	1	110
PRESENT	ABSENT	1	1	0	300
ABSENT	PRESENT	1	0	1	1200
ABSENT	ABSENT	1	0	0	4800

Note from the above table that if only the 110 Baud rate is required, pullup resistors on data lines D1, D2 and D7 represent the only external hardware required to select this data rate.

As shown in fig. 4, the INS8073 F1 flag is double buffered to

provide an RS-232 compatible voltage output and a 20 ma current output. The 20 ma current drive is produced by transistor switch Q1 and resistor R14. Positive and negative RS-232 levels are generated by the LM 747 op amp.

The INS8073 F2 flag is used to enable/disable the TTY reader relay via transistor switch Q2 and current limiting resistor R17. These components will supply 20 ma of current to a 12V (600Ω) relay.

The INS8073 will accept serialized ASCII input data on its SA/INTA input. As shown in fig. 4, the RS-232 input signal is selected via a jumper between E5-E6, or the TTY input signal may be selected via a jumper between E6-E7.

AUDIO CASSETTE HARDWARE INTERFACE

The INS8073 flag outputs allow data to be written directly onto audio cassette tape via an extremely low cost interface circuit. As shown in fig. 4, this circuit simply consists of 3 resistors, R28 - R30. These resistors form a simple voltage divider which is directly driven by the INS8073 flag outputs F2 and F3. The output from the voltage divider directly drives the microphone input to the cassette recorder.

Output data from the cassette recorder is received on the INS8073 SENSE B input, SB. As shown in fig. 4, only an inexpensive AC coupled transistor buffer (Q3) is required.

AUDIO CASSETTE RECORDING TECHNIQUE

The input waveform to the cassette microphone input is shown in fig. 7A. This waveform is used to represent a clock pulse and a data pulse. The waveform shown has the following desireable characteristics:

1) The peak excusion of the signal from its average value is approximately 60 MV.

2) When the signal is repeated, the average value of the repeated waveform is independent of the repetition rate.

3) The positive and negative excusions of the signal from the average value are equal. This prevents asymmetric distortion when the signal is recorded at a high volume level. (Many inexpensive cassette recorders do not allow adjustment of the recording level. Only the playback volume can be adjusted.)

4) Since the waveform is symmetric about the average value, tapes which are produced on one recorder may be played back on a different recorder. This may be done even though the recorders have record/playback circuitry which is 180 degrees out

6/7/79 RP

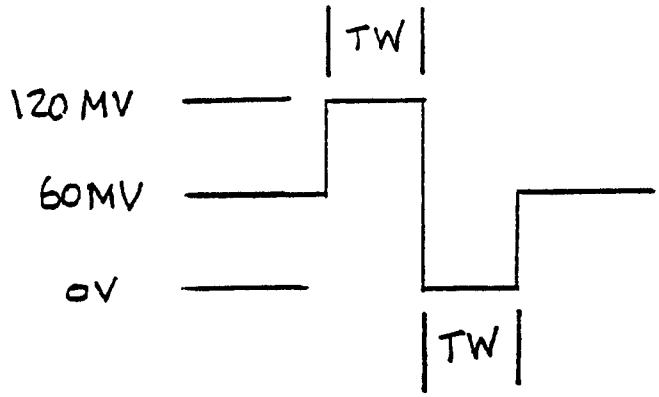


Fig. 7A Cassette Clock/Data Pulse

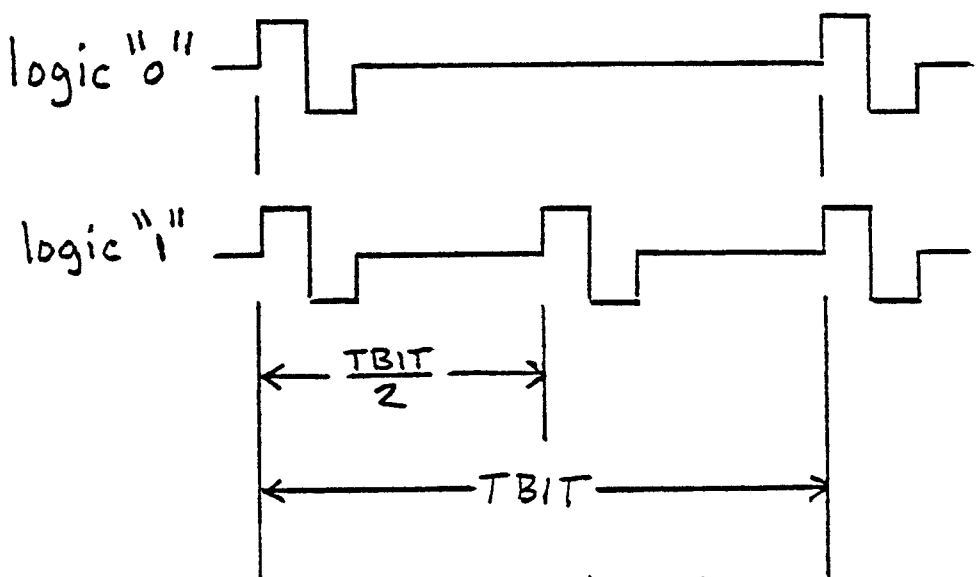


Fig 7B Cassette Data Waveforms

of phase. Because the recorded waveform is symmetric, logical inversion of the recorded data will not occurr when the recording scheme described below is employed.

Logical ones and zeros are recorded on the tape via an FM recording technique. As shown in fig. 7B, if the data bit to be written on the tape is a "1", it will be represented by a clock pulse followed by a data pulse. If data bit to be written is a "0", it will be represented by a clock pulse and the absence of a data pulse. This technique offers the advantage of providing clock synchronization for each data bit. Thus normal tape speed variations will not cause receipt of incorrect data.

The maximum data rate that can be recorded on the tape is a strong function of the recorder/tape frequency response. For even the poorest quality recorder/tape combination, a data rate of 500 Baud is readily achievable. If tapes are to be recorded and played back on the same good quality recorder, significantly higher data transfer rates can be readily achieved.

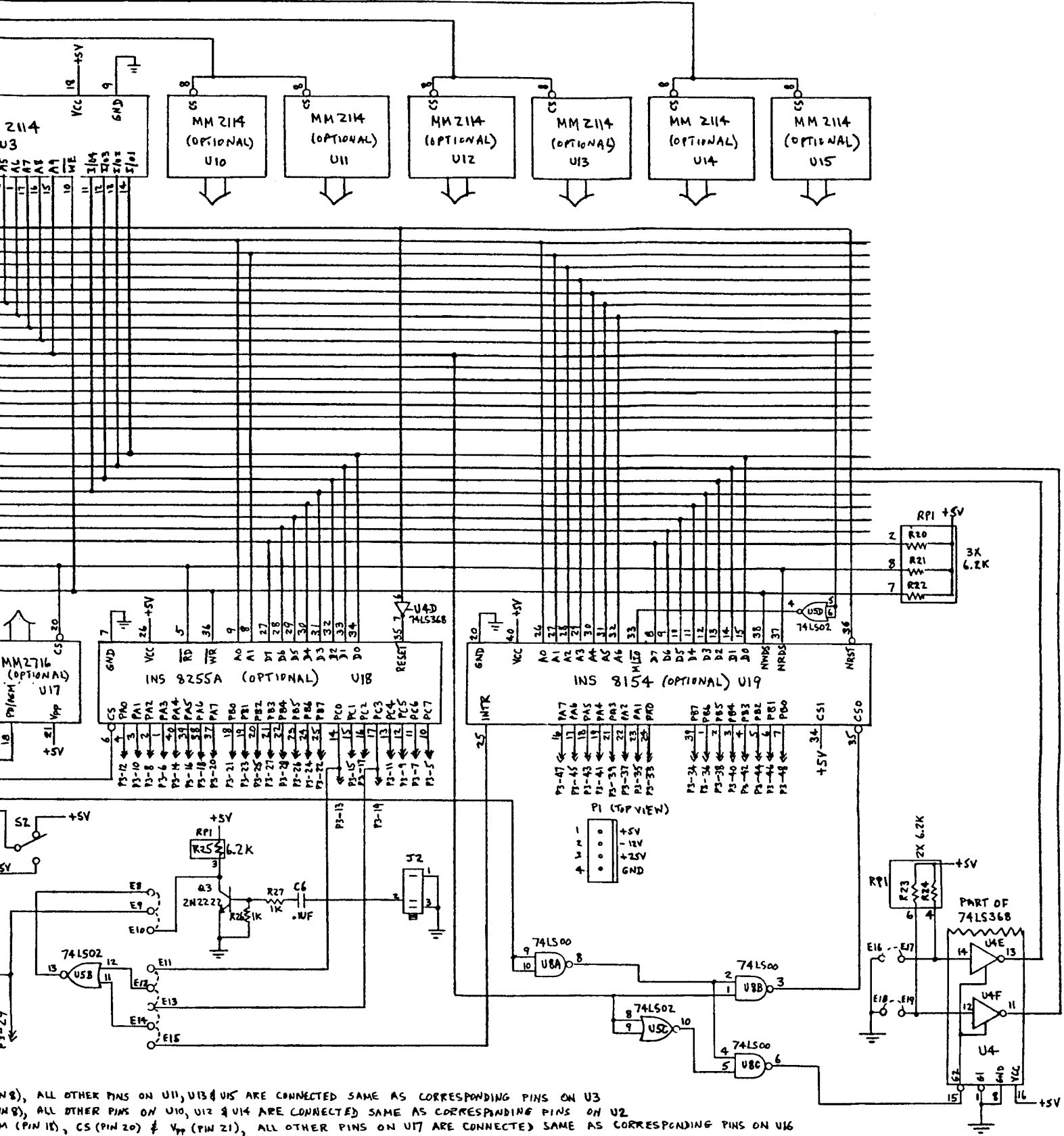
Head misalignment from recorder to recorder will sometimes cause problems to occurr when a tape is recorded on one machine and played back on another. These problems are the result of a low signal-to-noise ratio due to head misalignment, and can be minimized by choosing a slower data transfer rate, and/or aligning the azimuth angles of both recorders so that they are approximtely the same.

CONCLUSIONS

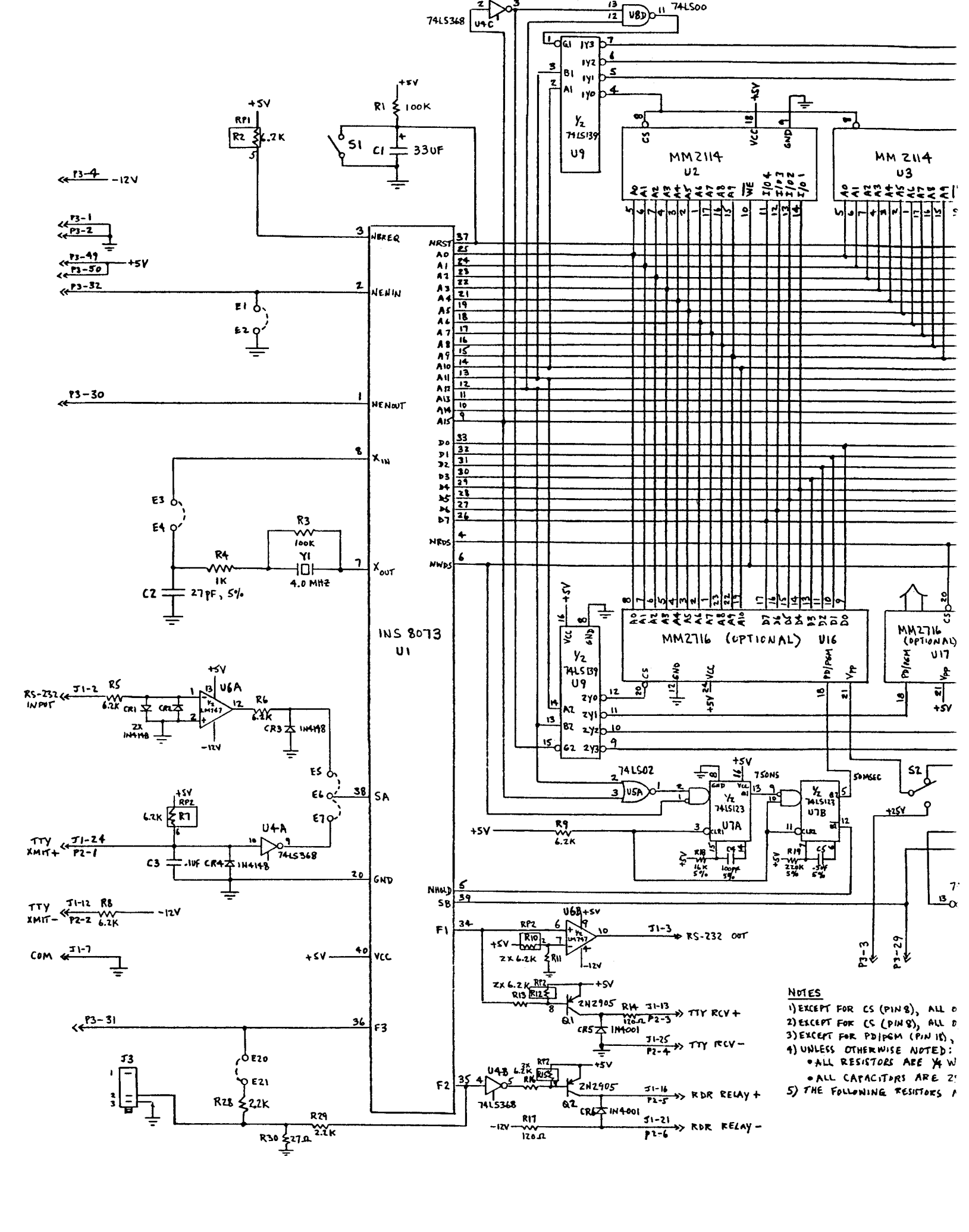
The INS8073 high level language processor may be employed in a broad spectrum of system applications. It offers the designer the power and convenience of a high level language, plus the cost effectiveness of a "minimum hardware" solution. Writing programs in a high level language is quick and easy, and enables the system designer to get his product to market more quickly.

NOTE:

AN EPROM RESIDENT "UTILITY" PROGRAM IS AVAILABLE FOR THE SYSTEM SHOWN IN FIG. 4. THE PROGRAM IS WRITTEN IN NIBL2, AND ALLOWS THE USER TO STORE/RETRIEVE CASSETTE PROGRAMS, PROGRAM MM2716 EPROMS, AND DOWNLOAD PROGRAMS FROM A "HOST" COMPUTER. A NUMBER OF OTHER FEATURES ARE ALSO INCLUDED. FOR ADDITIONAL DETAILS, REFER TO THE "NIBL2 CARD SYSTEM SOFTWARE" DESCRIPTION.

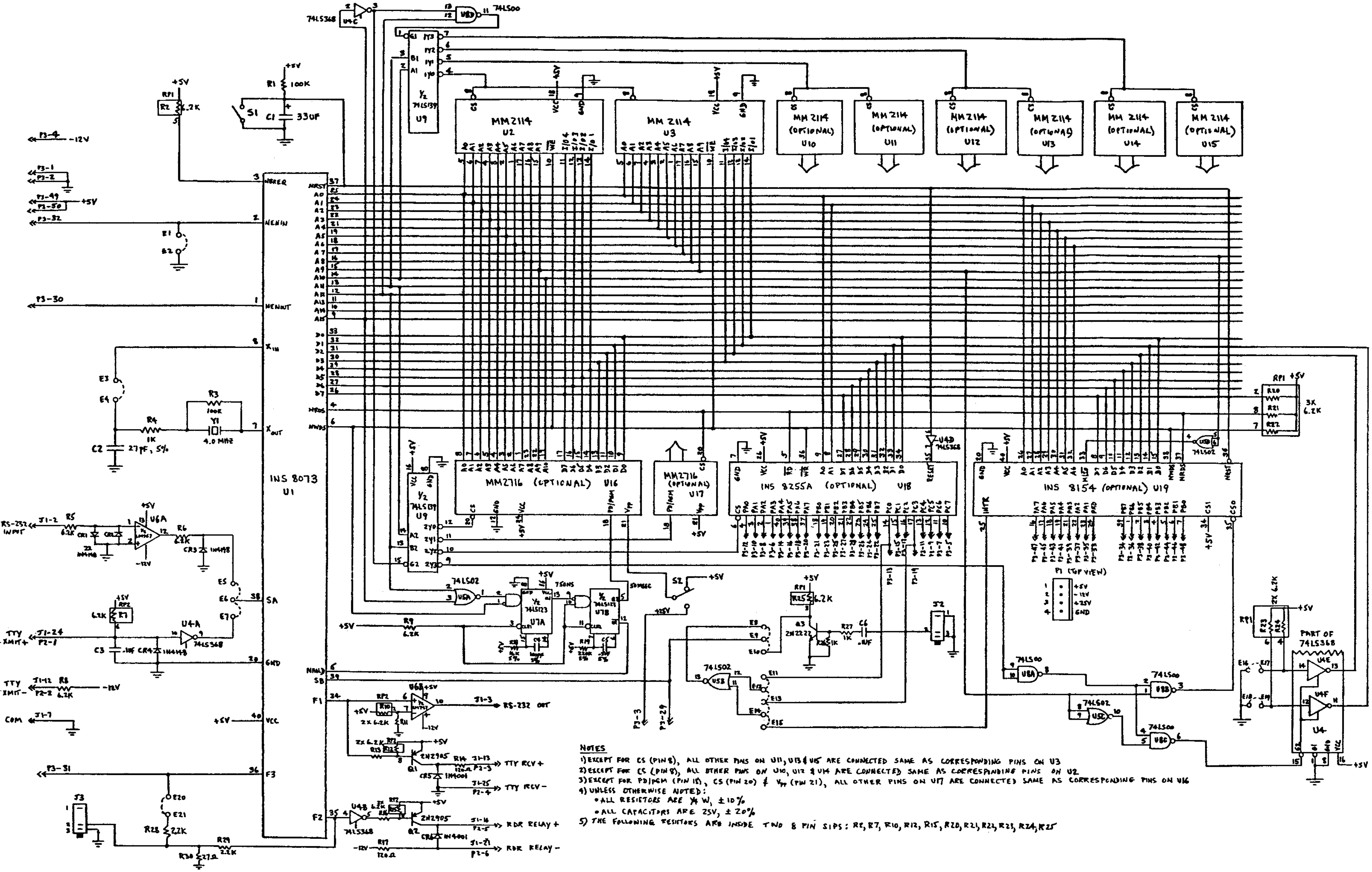


N8), ALL OTHER PINS ON U11, U13 & U15 ARE CONNECTED SAME AS CORRESPONDING PINS ON U3
N8), ALL OTHER PINS ON U10, U12 & U14 ARE CONNECTED SAME AS CORRESPONDING PINS ON U2
M (PIN 18), CS (PIN 20) & V_{pp} (PIN 21), ALL OTHER PINS ON U17 ARE CONNECTED SAME AS CORRESPONDING PINS ON U16
E NOTED:
ARE ¼ W, ±10%
RS ARE 25V, ±20%
RESISTORS ARE INSIDE TWO 8 PIN SIPS: R6, R7, R10, R12, R15, R20, R21, R22, R23, R24, R25



NOTES

1) EXCEPT FOR CS (PIN 8), ALL O
2) EXCEPT FOR CS (PIN 8), ALL D
3) EXCEPT FOR PD/PGM (PIN 18),
4) UNLESS OTHERWISE NOTED:
   • ALL RESISTORS ARE ¼ W
   • ALL CAPACITORS ARE 2
5) THE FOLLOWING RESISTORS A



NOTES

1) EXCEPT FOR CS (PIN 8), ALL OTHER PINS ON U11, U13 & U15 ARE CONNECTED SAME AS CORRESPONDING PINS ON U3
2) EXCEPT FOR CS (PIN 8), ALL OTHER PINS ON U10, U12 & U14 ARE CONNECTED SAME AS CORRESPONDING PINS ON U2
3) EXCEPT FOR PD/PGM (PIN 18), CS (PIN 20) & V_{PP} (PIN 21), ALL OTHER PINS ON U17 ARE CONNECTED SAME AS CORRESPONDING PINS ON U16
4) UNLESS OTHERWISE NOTED:
   - ALL RESISTORS ARE ¼ W, ± 10%
   - ALL CAPACITORS ARE 25V, ± 20%
5) THE FOLLOWING RESISTORS ARE INSIDE TWO 8 PIN SIPS: R2, R7, R10, R12, R15, R20, R21, R22, R23, R24, R25

FEATURE SUMMARY FOR INS8073 SYSTEM CARD

HARDWARE FEATURES

* DIRECTLY INTERFACES TO:

  1) RS-232 TERMINAL AT 4 SELECTABLE DATA RATES - 4800, 1200, 300 AND 110 BAUD
  2) TTY AT 110 BAUD
  3) INEXPENSIVE CASSETTE RECORDER FOR STORAGE/RETRIEVAL OF NIBL2 SOURCE PROGRAMS AND ASSEMBLY LANGUAGE LM'S

* ON CARD PROGRAMMER FOR MM2716 EPROMS

* 1K RAM PROGRAM MEMORY PLUS OPTIONAL 3K RAM PROGRAM MEMORY

* OPTIONAL 4K EPROM PROGRAM MEMORY

* I/O CAPABILITY CONSISTS OF:

  1) TWO SENSE/INTERRUPT INPUTS & 3 FLAG OUTPUTS
  2) 40 I/O LINES FROM OPTIONAL INS8255 AND INS8154 (INCLUDES 128 BYTES OF SCRATCHPAD RAM)
  3) THREE USER SELECTABLE, NIBL2 SUPPORTED VECTORED INTERRUPTS

* THE MINIMUM SYSTEM CONSISTS OF 9 IC'S AND MAY BE EXPANDED, ON CARD, UP TO 19 IC'S

SOFTWARE FEATURES

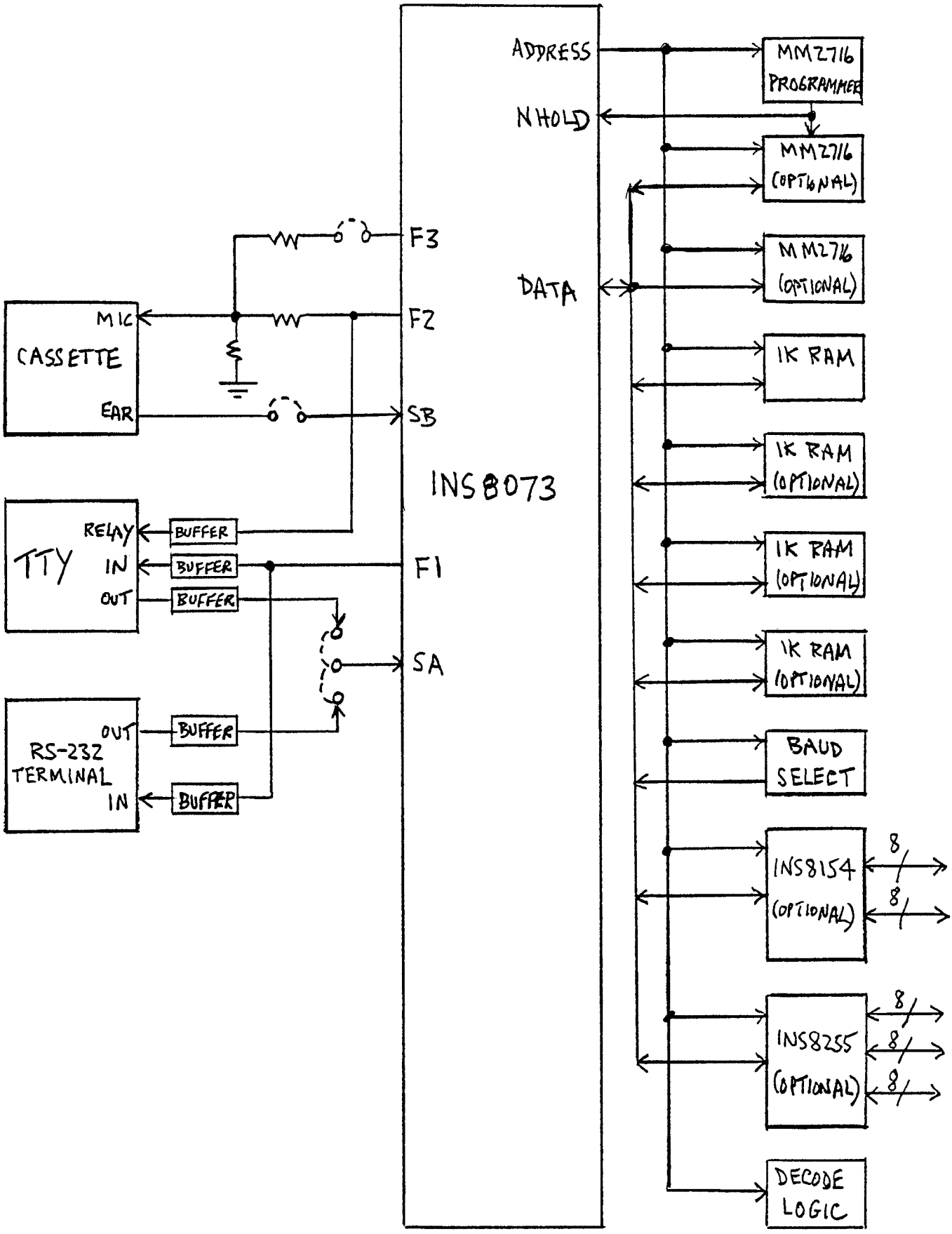
* AUTOMATIC POWER-ON EXECUTION OF USER'S EPROM PROGRAM FOR REAL TIME CONTROL APPLICATIONS (NO TERMINAL REQUIRED)

* LINK CAPABILITY TO ASSEMBLY LANGUAGE SUBROUTINES FROM NIBL2 PROGRAMS AND DIRECT EXECUTION OF ASSEMBLY LANGUAGE PROGRAMS AT POWER-ON

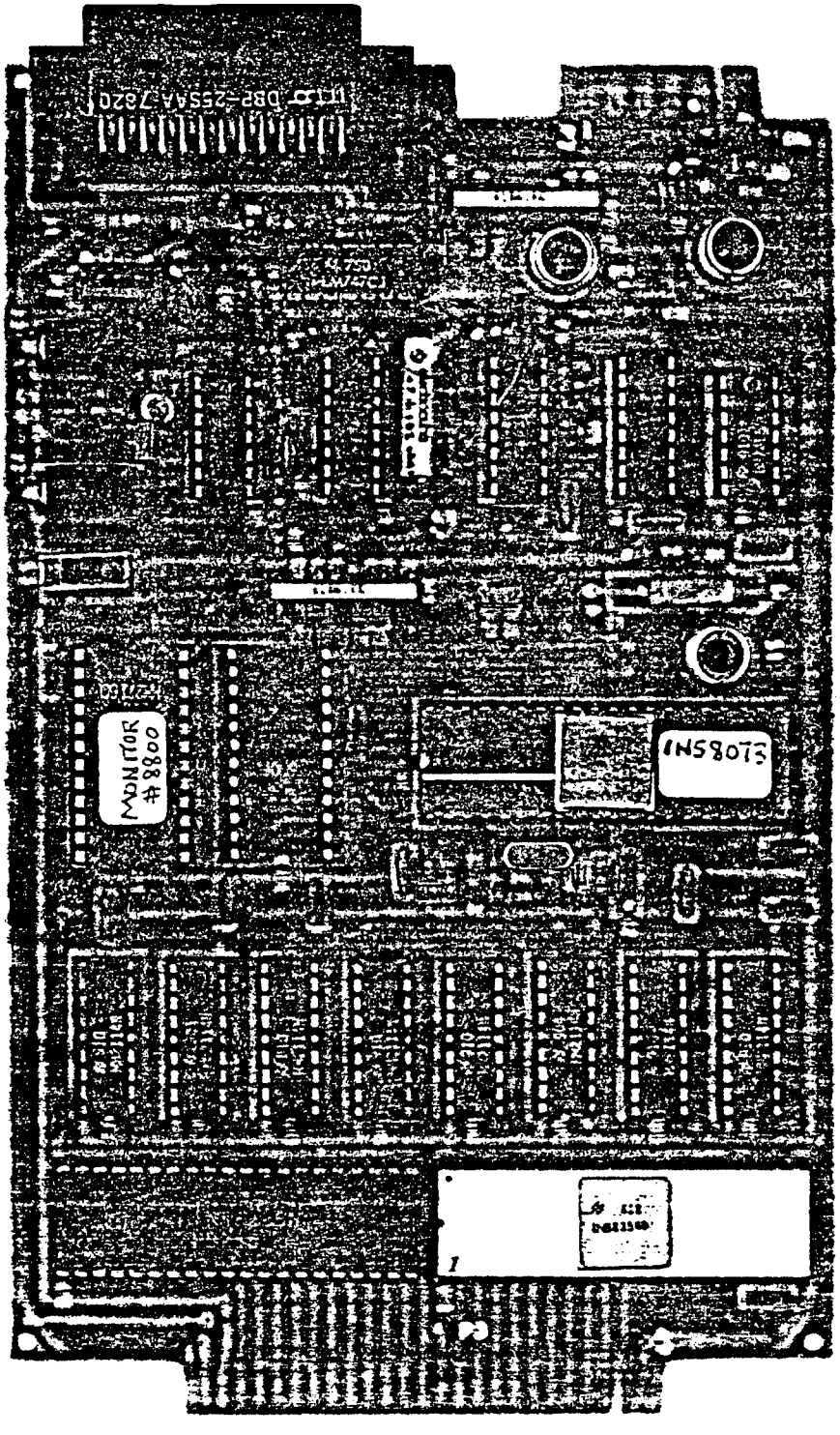
* USER PROGRAMS MAY BE STORED ON PAPER TAPE, CASSETTE, EPROM, OR DOWNLOADED AT 4800 BAUD FROM A "HOST" COMPUTER (PACE UDS, STARPLEX, ETC.)

* EPROM RESIDENT UTILITY PROGRAM SUPPORTS THE FOLLOWING COMMANDS:

  P - PROGRAM 2716 EPROM FROM SPECIFIED MEMORY RANGE
  W - WRITE SPECIFIED MEMORY RANGE ONTO CASSETTE
  R - READ CASSETTE RESIDENT PROGRAM INTO MEMORY WITH OPTIONAL DISPLACEMENT
  L - LOAD ASCII ENCODED PAPER TAPE LM INTO MEMORY AT 110 BAUD WITH OPTIONAL DISPLACEMENT
  A - ACCEPT DOWNLOADED NIBL2 SOURCE PROGRAM OR ASSEMBLY LANGUAGE LM WITH OPTIONAL DISPLACEMENT AT 4800 BAUD
  D - DUMP CONTENTS OF SPECIFIED MEMORY RANGE IN HEX/ASCII FORMAT
  C - COPY CONTENTS OF SPECIFIED MEMORY RANGE (RAM/EPROM) TO SPECIFIED RAM DESTINATION
  V - VERIFY CONTENTS OF 1ST MEMORY RANGE AGAINST 2ND MEMORY RANGE
  F - FILL A SPECIFIED MEMORY RANGE WITH A SPECIFIED BYTE
  E - ERASURE TEST FOR A SPECIFIED MEMORY RANGE (TEST THAT MEMORY RANGE IS FILLED WITH A SPECIFIED BYTE)



BLOCK DIAGRAM OF INS8073 SYSTEM CARD


MONITOR
#8800
8085N1